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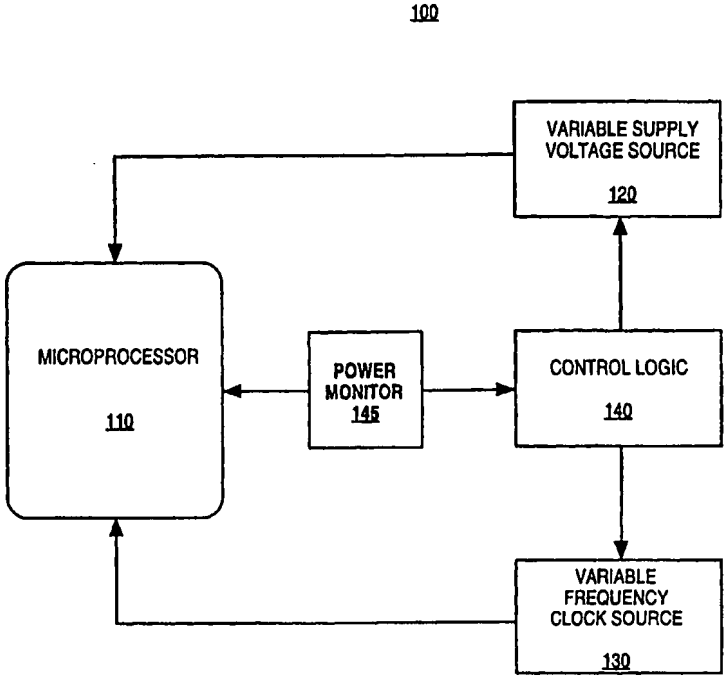
(54) Title: METHOD AND APPARATUS FOR POWER THROTTLING IN A MICROPROCESSOR USING A CLOSED LOOP FEEDBACK SYSTEM

(57) Abstract

A method and apparatus for power throttling in a microprocessor (110). A voltage source (120) supplies voltage to the microprocessor (110), and a clock source (130) operates the microprocessor (110) at a desired frequency. A power monitor (145) or alternatively a temperature sensor is configured to measure the short term power consumption or temperature of the microprocessor (110). Control logic (140) is coupled to the voltage source (120) and the clock source (130). The control logic (140) receives an indication of the power consumption or temperature, as applicable, and compares to a predetermined threshold. In response to the comparison, the control logic (140) varies the supply voltage and the frequency.



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METHOD AND APPARATUS FOR POWER THROTTLING IN A MICROPROCESSOR USING A CLOSED LOOP FEEDBACK SYSTEM

1. FIELD OF THE INVENTION

The present invention relates generally to computer systems architecture, and, more particularly, to a method and apparatus for power throttling in a microprocessor system using a closed loop feedback system.

2. DESCRIPTION OF THE RELATED ART

The clock speed of microprocessors has increased dramatically over the past several years. In the early eighties, microprocessors had clock speeds typically ranging from 5 to 16 MHz, which was sufficient to handle computer applications during that time period. However, as computer applications became more complex over the years to meet the demands of the computer user, the sluggish processor speeds of the past did not suffice. Today, microprocessors have clock speeds far exceeding those of the past, running at more than 300 MHz. And, these clock speeds show no sign of reaching a pinnacle. The microprocessors of the not-to-distant future have projected clock speeds that will significantly dwarf today's clock speed standards. With these higher clock speeds, microprocessors are capable of handling more and more complex computer applications in shorter periods of time, thus providing inherent benefits to the computer user.

Although the dramatic increase in the microprocessor's clock speed over the years has enabled the computer user to run more complex computer applications at faster speeds, it has posed problems for the computer systems designer. Such a significant increase in clock speed causes a substantial increase in the power consumed by the microprocessor, thus requiring the need for larger and more powerful power supplies. As the peak power of the microprocessor has increased to meet this demand for

increased clock speed, the spread between the peak power and the average power that is typically consumed by the microprocessor has significantly increased as well.

Generally, a computer system is designed to account for the peak power consumed by the computer using higher delivery power supplies and adequate cooling devices to dissipate the peak power, even though this peak power consumption is seldom realized. This "overdesign" places unnecessary guard bands in the power and thermal design of the computer, thus increasing its cost and placing various limitations on the computer user. That is, a larger power supply adds weight and increases the size of the computer, which is particularly disadvantageous to the user of a portable computer, for example.

One method used to control the power consumption of a microprocessor is to adjust the effective frequency (i.e., clock speed) of the microprocessor to reduce the power. Since power is a linear function of the clock speed, the power reduces linearly with a decrease in the clock speed.

The present invention is directed to overcoming, or at least reducing the effects of, one or more of the problems set forth above.

SUMMARY OF THE INVENTION

In one aspect of the present invention, a method for power throttling in a microprocessor having a voltage source and a clock applied thereto is provided. The method includes monitoring the short term power consumption of the microprocessor, comparing the power consumption to a predetermined value, and varying the clock speed and the supply voltage of the microprocessor in response to the comparison. In an alternative embodiment, the temperature of the microprocessor is the measured variable, rather than the short term power consumption. In such an embodiment, the measured temperature is compared to a predetermined value, and in response thereto, the clock speed and supply voltage are varied.

In another aspect of the invention, a power throttling device includes a microprocessor, a voltage source to supply voltage to the microprocessor, a clock source

to operate the microprocessor at a desired frequency, and a power monitor configured to measure the short term power consumption of the microprocessor. Control logic is coupled to the voltage source and the clock source. The control logic adapted to receive an indication of the power consumption from the power monitor and compare the power consumption to a predetermined value, and in response to the comparison, vary the supply voltage and the frequency. In an alternative embodiment, a temperature sensor is provided in place of the power monitor to measure the temperature of the microprocessor. The control logic receives an indication of the measured temperature from the temperature sensor and compares it to a predetermined value. In response to the comparison, the control logic varies the supply voltage and the frequency.

BRIEF DESCRIPTION OF THE DRAWING

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

Figure 1 is a block diagram of a power throttling closed loop feed back system in accordance with an embodiment of the present invention, in which power consumption is the measured variable in the closed loop feed back system;

Figure 2 is a block diagram of a power throttling closed loop feed back system in accordance with another embodiment of the present invention, in which temperature is the measured variable in the closed loop feed back system;

Figure 3 is a block diagram of a power throttling closed loop feedback system in accordance with yet another embodiment of the present invention, in which various components of the system are integral with a microprocessor;

Figure 4 shows an alternative embodiment of the power throttling closed loop feedback system illustrated in Figure 3;

Figure 5 shows a process for power throttling in accordance with an embodiment of the present invention, which may be performed by a control logic of Figures 1 - 4;

Figure 6 shows a process for power throttling in accordance with a specific embodiment of the present invention, in which temperature is the measured variable in the closed loop feed back system; and

Figure 7 shows a process for power throttling in accordance with another specific embodiment of the present invention, in which short term power consumption is the measured variable in the closed loop feed back system.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nonetheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

Turning now to the drawings, and specifically referring to Figure 1, a block diagram of a power throttling closed loop feedback system 100 is shown in accordance with one embodiment of the present invention. The system 100 includes a microprocessor 110, which, in accordance with one embodiment, is a Pentium® II processor manufactured and sold by Intel Corporation of Santa Clara, California.

However, it will be appreciated that the microprocessor 110 could be any type of commercially available processor, and, thus need not be limited to any one specific type.

In accordance with one embodiment, the system 100 is part of a computer system (not shown), such as a personal computer (PC). However, it will also be appreciated that the system 100 could be employed in various other types of systems or devices, which would use the microprocessor 110 to control their functions, without departing from the spirit and scope of the present invention.

The system 100 further includes a supply voltage source 120, which is coupled to the microprocessor 110 to supply power thereto. In one embodiment, the voltage source 120 is a variable voltage source comprising a conventional switching voltage regulator. A clock source 130 also is coupled to the microprocessor 110 to control the frequency (i.e., clock speed) of the microprocessor 110. In accordance with one embodiment, the clock source 130 frequency is variable, and may be constructed using a phase locked loop (PLL).

Control logic 140 is coupled to both the variable supply voltage source 120 and the variable frequency clock generator 130 to control the operation of these devices. The system 100 also includes a power monitoring device 145 that is configured to measure the short term power consumption of the microprocessor 110. The power consumption measurement is considered short term as compared to the power consumption rate of change. In one embodiment, the power monitoring device 145 includes a known resistance coupled between the voltage source 120 and the microprocessor 110. Power consumption may be determined based on the voltage across the resistance and knowledge of the voltage provided by the voltage source 120. This is but one exemplary power monitoring scheme. One skilled in the art having the benefit of this disclosure may employ other means for monitoring power consumption of the microprocessor 110.

Another embodiment of a system 105 in accordance with the present invention is illustrated in Figure 2. A temperature sensor 150 monitors a temperature T_d of the microprocessor 110. In accordance with a particular embodiment, the temperature sensor 150 measures the temperature of the silicon die (not shown) that includes the integrated

circuitry of the microprocessor 110. In an alternative embodiment, the temperature sensor 150 could also be configured to measure the temperature of the package case (not shown) that surrounds the silicon die of the microprocessor 110. Although the temperature of the silicon die and the package case of the microprocessor 110 are directly related, it is desirable to measure the temperature of the die for a more accurate temperature reading.

The microprocessor 110 is capable of running various types of commercially available computer applications thereon. Typically, more complex operations performed by the microprocessor 110, when running a particular application, will cause the power consumption and the temperature T_d of the microprocessor 110 to increase. For example, if the microprocessor 110 has a three-dimensional graphics application running thereon, it typically will work harder to process the more complex operations that are required by the 3D graphics application. However, when the microprocessor 110 is running a word-processing application, for example, the microprocessor 110 may not endure any complex processing (especially when compared to that of the 3D graphics application). Accordingly, as the microprocessor 110 works harder to process more complex operations (such as complex 3D graphics), the power consumption and temperature T_d of the microprocessor 110 will generally rise. And, when the microprocessor 110 processes less complex operations (such as word-processing, for example), the power consumption and temperature T_d of the microprocessor 110 will typically fall.

The control logic 140 monitors such rising and falling of the microprocessor's power consumption, or, in the embodiment illustrated in Figure 2, the temperature T_d. The control logic 140 is operable to compare the power consumption or temperature T_d to a predetermined value, and in response thereto, affect the voltage source 120 and the clock source 130 to vary the clock speed and the supply voltage. For instance, the clock speed and supply voltage may be varied in response to the power consumption or temperature T_d exceeding, or approaching, the predefined value. Particularly, for throttling microprocessor 110, the clock speed and supply voltage are reduced in

response to the power consumption or temperature T_d exceeding, or approaching, the predefined value.

In some embodiments, the comparison to a predefined value comprises comparing the measured variable to a predefined range. For example, referring to Figure 2, when the temperature T_d of the microprocessor 110 rises above an optimal operating range T_1 - T_2 for the microprocessor 110, the control logic 140 will send a control signal to the variable frequency clock source 130 to decrease the frequency of the microprocessor 110. This will effectively slow down the clock speed of the microprocessor 110, which will cause the temperature T_d of the microprocessor 110 to fall closer to, if not within, the optimal temperature range T_1 - T_2 of the microprocessor 110. The optimal temperature range T_1 - T_2 is predetermined and set by the system designer of the computer, in which the system 105 is a part.

While the microprocessor 110 is running at a reduced clock speed, the microprocessor 110 will typically not require as much power from the variable supply voltage source 120 as it did when it was running at the higher clock speed. Accordingly, the control logic 140 will also send a control signal to the variable supply voltage source 120 to reduce the power supplied to the microprocessor 110 such that enough power is supplied to have the microprocessor 110 run at the lower clock speed. By lowering the supply voltage, less power is consumed, which would be particularly beneficial if the system 105 were employed in a mobile or portable environment such as a laptop computer, for example.

As power is a linear function of frequency, reducing the clock speed (frequency) of the microprocessor results in a linear reduction in power consumption. However, since power has a quadratic relationship with supply voltage, varying both supply voltage in addition to varying the clock speed provides a significant power saving, as compared to power throttling by reducing frequency alone.

In particular embodiments, if the temperature sensor 150 measures the temperature T_d of the microprocessor 110 to be below the lower limit T_1 of the optimal temperature range T_1 - T_2, then the control logic 140 will send a control signal to increase

the output of the variable supply voltage source 120 to adequately accommodate an anticipated increase in the clock speed of the microprocessor 110. Subsequently, the control logic 140 will also send a control signal to the variable frequency clock source 120 to increase the clock speed of the microprocessor 110, such that the temperature T_d of the microprocessor 110 rises closer to, if not within, the optimal temperature range T_1 - T_2. Due to the anticipated increase in clock speed of the microprocessor 110, the control logic 140 increases the supply voltage of the variable supply voltage source 120 to accommodate the subsequent increase in clock speed.

The control logic 140 has the temperature sensor continuously monitor the temperature T_d of the microprocessor 110 such that the adjustments to the variable frequency clock source 130 and the variable supply voltage source 120 can be continually made to keep the microprocessor 110 operating within the optimal temperature range T_1 - T_2. Hence, by controlling the system temperature, the cost of the system can be reduced because the necessity to overdesign the system with additional cooling for the peak power consumption has been eliminated.

Turning now to Figures 3 and 4, block diagrams of power throttling closed loop feedback systems 200 and 205, respectively, are shown in accordance with embodiments of the present invention. In the particular embodiments illustrated in Figures 3 and 4, the power monitor 145 (Figure 3) or temperature sensor 150 (Figure 4), variable frequency clock source 130, and control logic 140 are all integrated on the die of the microprocessor 110. Of course, the variable supply voltage source 120 cannot be an integral part of the microprocessor 110 due to its physical size, and, thus remains as a separate component from the microprocessor 110. The microprocessor 110 further includes other microprocessor circuitry 210, as is well established in the art, to control the aspects of the computer system, for example.

In Figure 5, a process 250 for power throttling in a microprocessor in accordance with the present invention is illustrated. In step 260, either the short term power consumption or the temperature of the microprocessor 110 is monitored. In step 270, the power consumption or temperature is compared to a predetermined value, and in

step 280 the clock speed and supply voltage are varied based on the comparison of step 270. Particularly, if the comparison of step 270 determines that the measured variable exceeds, or is approaching the predetermined value, the clock speed and supply voltage are adjusted to affect the measured variable -- power consumption or temperature.

Turning now to Figure 6, an exemplary process 300 for performing the power throttling technique as performed by the control logic 140 is shown. The process 300 commences at step 310, where the control logic 140 determines the temperature T_d of the microprocessor 110 via the temperature sensor 150. As previously mentioned, the temperature sensor 150 could monitor the temperature T_d of the die directly or, in the alternative, of the package case that surrounds the microprocessor 110. Next, at step 320, the control logic 140 determines if the temperature T_d of the microprocessor 110 is outside of the optimal temperature operating range T_1 - T_2 of the microprocessor 110. If the temperature T_d of the microprocessor 110 is within the temperature range T_1 - T_2, the process 300, reverts back to step 310, where the control logic 140 again determines the temperature T_d of the microprocessor 110 via the temperature sensor 150. On the other hand, if the temperature T_d of the microprocessor 110 falls outside of the optimal temperature range T_1 - T_2, then the process 300 advances to step 330, where the control logic 140 determines if the temperature T_d of the microprocessor 110 is greater than the upper limit (i.e., T_2,) of the temperature range T_1 - T_2.

If the temperature T_d of the microprocessor 110 is greater than the upper limit temperature T_2, then at step 340 the control logic 140 sends a control signal to the variable frequency clock generator 130 to lower the clock speed of the microprocessor 110 by a predetermined amount. Subsequent to lowering the clock speed at step 340, the control logic 140 sends a control signal to the variable supply voltage source 120 at step 350 to lower the supply voltage to the microprocessor 110 to conserve power. Subsequent to adjusting the variable supply voltage 120 (at step 350), the process 300 reverts back to step 310, where the temperature T_d of the microprocessor 110 is again measured by the temperature sensor 150.

If the temperature T_d of the microprocessor 110 is not above the upper limit T_2 at step 330. Then it is assumed by the control logic 140 that the temperature T_d of the microprocessor 110 is below the lower limit T_1. If the temperature T_d is below the lower limit T_1 the process 300 proceeds to step 360, where the supply voltage of the variable supply voltage source 120 is raised to accommodate the anticipated increase in the clock speed of the microprocessor 110. Subsequently, at step 370, the control logic 140 sends a control signal to the variable frequency clock source 130 to increase the clock speed of the microprocessor 110, which will raise the temperature T_d closer to, or within, the optimal temperature range T_1 - T_2. Subsequent to adjusting the clock speed of the microprocessor 110, the process 300 reverts back to step 310, where the temperature T_d of the microprocessor 110 is measured again by the temperature sensor 150. The particular process disclosed above in conjunction with Figure 5, using two threshold temperatures, is exemplary only. Other feedback control systems may be employed to accomplish the power throttling technique illustrated in Figure 6 without departing from the spirit of the present invention.

Referring now to Figure 7, another process 400 for performing the power throttling technique as performed by the control logic 140 is illustrated. The process 400 is similar to the process shown in Figure 6, except short term power consumption P_d is measured, rather than the temperature of the microprocessor. In step 410 the control logic 140 determines the short term power consumption P_d using a power monitoring device such as the power monitor 145 described herein above. As disclosed above, the measurement is considered short term as compared to the rate of change of the measured variable. At step 420, the control logic 140 determines if the power consumption P_d is outside of an optimal power consumption range $P_1 - P_2$. If the power consumption P_d falls outside of the optimal power consumption range $P_1 - P_2$, then the process 400 advances, and in step 430, the control logic 140 determines whether the power consumption P_d of the microprocessor 110 is above the power consumption range $P_1 - P_2$. Based on the determination of step 430, the clock speed and voltage are decreased (steps 440, 450) or increased (steps 460, 470). If, in step 420, the power consumption

P_d of the microprocessor 110 is within the power consumption range $P_1 - P_2$, the process 400 reverts back to step 410.

Example applications for the power monitoring apparatus and processes of the present invention include programmable battery life for a portable PC. If a user has a requirement for a portable PC to operate for a desired time period (a three-hour flight, for example), the portable PC's microprocessor may be programmed to run as fast as possible, but last for the entire time period. The system disclosed herein could then monitor the power consumption of the portable PC's microprocessor and adjust it to maintain the desired battery life, while running as fast as possible within this constraint. In another application, a computer system's cost may be reduced by using a less powerful power supply and a less extensive cooling system in conjunction with the throttling processes and apparatus disclosed herein.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED IS:

1. A method for power throttling in a microprocessor, the microprocessor having a voltage source and a clock applied thereto, the method comprising:

monitoring the short term power consumption of the microprocessor;

comparing the power consumption to a predetermined value; and

varying the clock speed and the supply voltage of the microprocessor in response to the comparison.

2. The method of claim 1, wherein the voltage source provides a known voltage, wherein monitoring the short term power consumption comprises:

providing a known resistance between the microprocessor and the voltage source; and

monitoring the voltage across the known resistance.

3. The method of claim 1, wherein varying the clock speed and the supply voltage of the microprocessor in response to the comparison comprises:

varying the clock speed and the supply voltage of the microprocessor in response to the power consumption exceeding the predetermined value.

4. The method of claim 1, wherein varying the clock speed and the supply voltage of the microprocessor in response to the comparison comprises:

varying the clock speed and the supply voltage of the microprocessor in response to the power consumption approaching the predetermined value.

5. A method for power throttling in a microprocessor, the microprocessor having a voltage source and a clock applied thereto, the method comprising:

determining the temperature of the microprocessor;

comparing the temperature to a predetermined value; and

varying the clock speed and the supply voltage of the microprocessor in response to the comparison.

6. The method of claim 5, wherein comparing the temperature to a predetermined value comprises determining whether the temperature is outside of a predetermined temperature range.

7. The method of claim 6, wherein determining whether the temperature is outside the predetermined temperature range comprises:

determining whether the temperature is above an upper limit of the predetermined temperature range.

8. The method of claim 6, wherein determining whether the temperature is outside the predetermined temperature range further comprises:

determining whether the temperature is below a lower limit of the predetermined temperature range.

9. The method of claim 5, wherein varying the clock speed and the supply voltage comprises:

reducing the clock speed and the supply voltage in response to the temperature exceeding the predetermined value.

10. The method of claim 5, wherein varying the clock speed and the supply voltage comprises:

reducing the clock speed and the supply voltage in response to the temperature approaching the predetermined value.

11. The method of claim 6, wherein varying the clock speed and the supply voltage comprises:

increasing the clock speed and the supply voltage in response to the temperature of the microprocessor being below a lower limit of the predetermined temperature range.

12. A power throttling device, comprising:

a microprocessor;

a voltage source to supply voltage to the microprocessor;

a clock source to operate the microprocessor at a desired frequency;

a power monitor configured to measure the short term power consumption of the microprocessor; and

control logic coupled to the voltage source and the clock source, the control logic adapted to receive an indication of the power consumption from the power monitor and compare the power consumption to a predetermined value, and in response to the comparison, vary the supply voltage and the frequency.

13. The power throttling device of claim 12, wherein the control logic is further operable to reduce the supply voltage and frequency in response to the power consumption exceeding the predetermined value.

14. The power throttling device of claim 12, wherein the control logic is further operable to reduce the supply voltage and frequency in response to the power consumption approaching the predetermined value.

15. The power throttling device of claim 12, wherein the clock source, the power monitor, and the control logic are all an integral part of the microprocessor.

16. The power throttling device of claim 12, wherein the clock source comprises a phase locked loop.

17. The power throttling device of claim 12, wherein the voltage source comprises a switching voltage regulator.

18. The power throttling device of claim 12, wherein the power monitor includes a known resistance coupled between the voltage source and the microprocessor.

19. A power throttling device, comprising:

a microprocessor;

a voltage source to supply voltage to the microprocessor;

a clock source to operate the microprocessor at a desired frequency;

a temperature sensor to measure the temperature of the microprocessor; and

control logic coupled to the voltage source and the clock source, the control logic adapted to receive an indication of the measured temperature from the temperature sensor and compare the temperature to a predetermined value, and in response to the comparison, vary the supply voltage and the frequency.

20. The power throttling device of claim 19, wherein the control logic is further operable to reduce the supply voltage and frequency in response to the temperature exceeding the predetermined value.

21. The power throttling device of claim 19, wherein the control logic is further operable to reduce the supply voltage and frequency in response to the temperature approaching the predetermined value.

22. The power throttling device of claim 19, wherein the clock source, the temperature sensor, and the control logic are all an integral part of the microprocessor.

23. The power throttling device of claim 19, wherein the clock source comprises a phase locked loop.

24. The power throttling device of claim 19, wherein the voltage source comprises a switching voltage regulator.

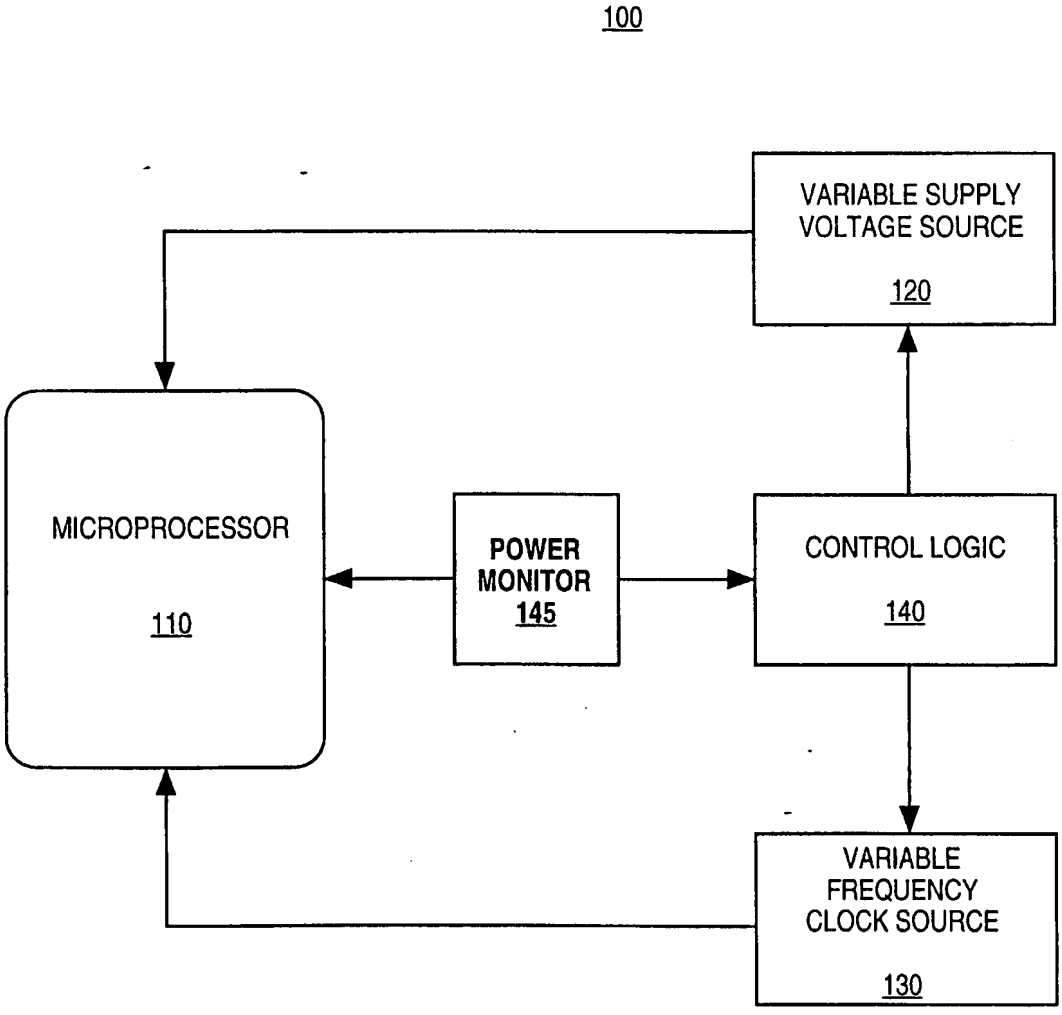
100
VARIABLE SUPPLY VOLTAGE SOURCE
120
MICROPROCESSOR
110
POWER MONITOR
145
CONTROL LOGIC
140
VARIABLE FREQUENCY CLOCK SOURCE
130

FIG. 1

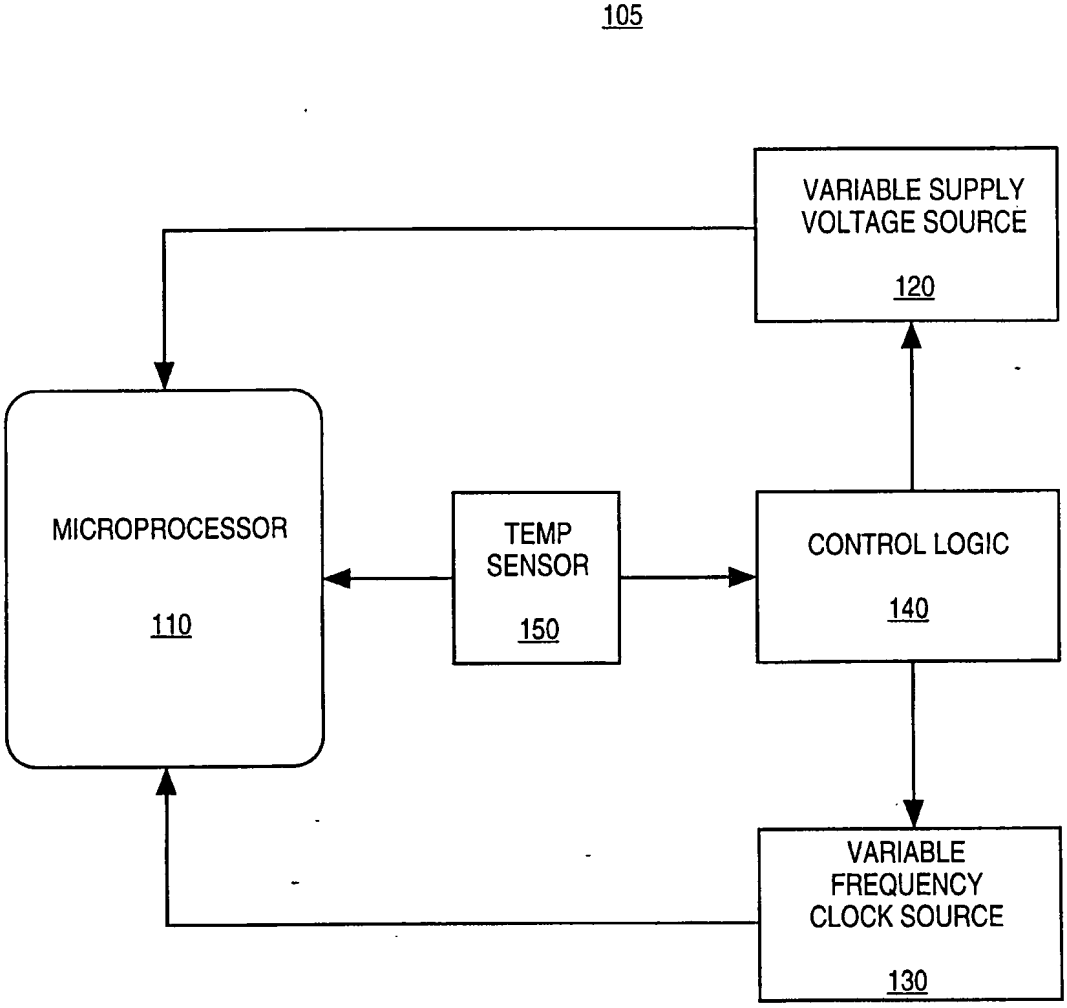
105
VARIABLE SUPPLY VOLTAGE SOURCE
120
MICROPROCESSOR
110
TEMP SENSOR
150
CONTROL LOGIC
140
VARIABLE FREQUENCY CLOCK SOURCE
130

FIG. 2

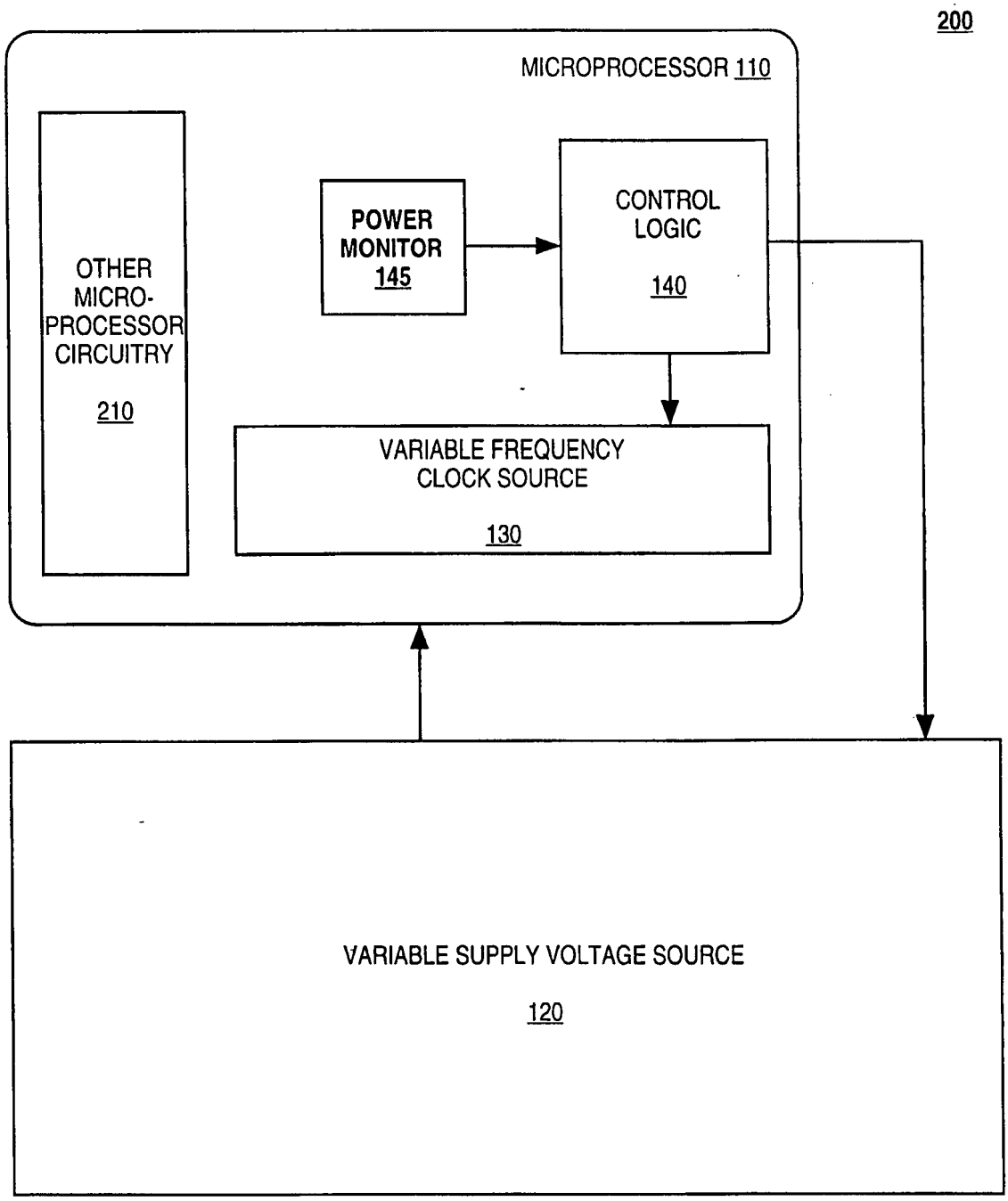
200
MICROPROCESSOR 110
OTHER MICRO-PROCESSOR CIRCUITRY 210
POWER MONITOR 145
CONTROL LOGIC 140
VARIABLE FREQUENCY CLOCK SOURCE 130
VARIABLE SUPPLY VOLTAGE SOURCE 120

FIG. 3

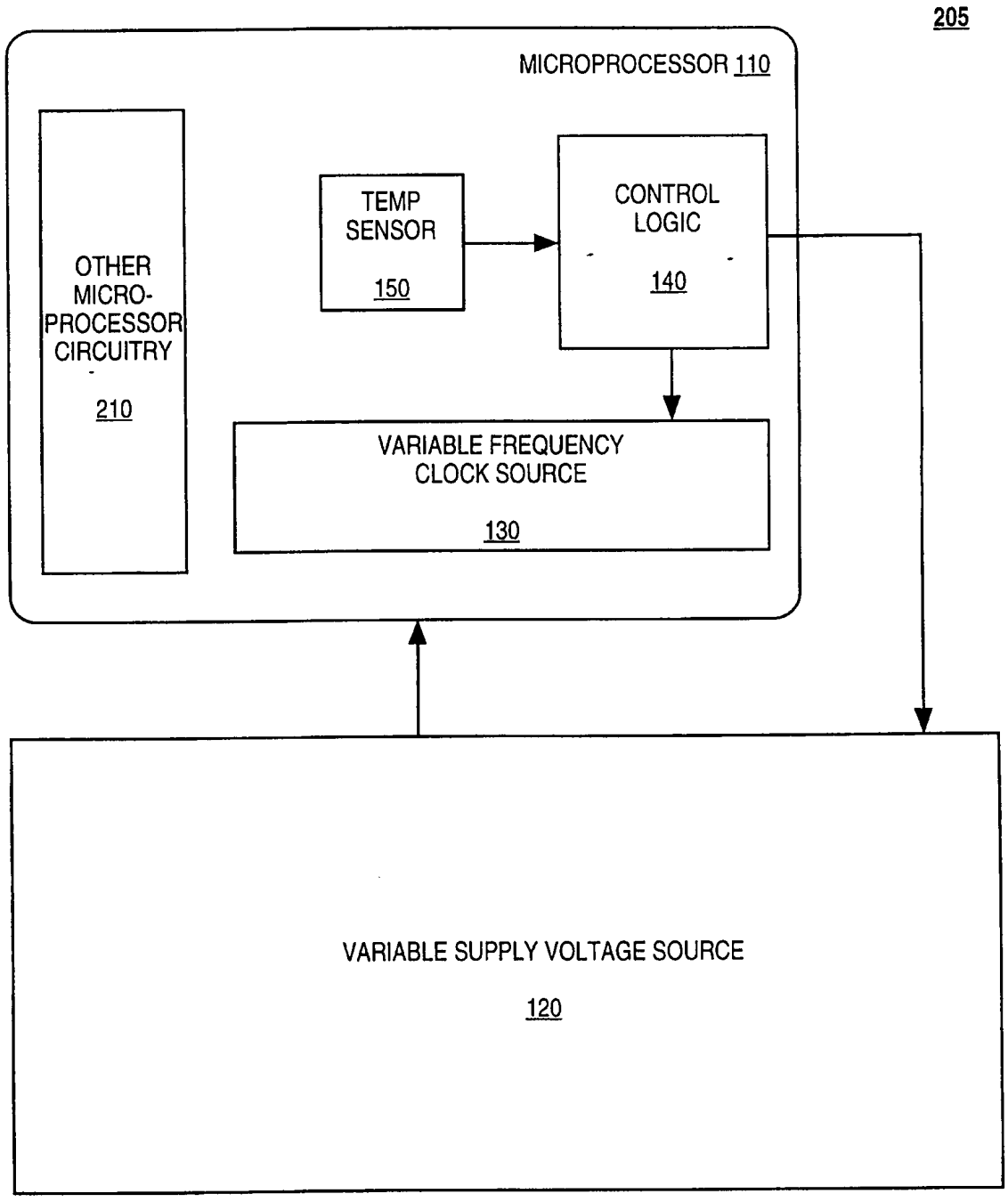
205
MICROPROCESSOR 110
OTHER MICRO-PROCESSOR CIRCUITRY 210
TEMP SENSOR 150
CONTROL LOGIC 140
VARIABLE FREQUENCY CLOCK SOURCE 130
VARIABLE SUPPLY VOLTAGE SOURCE 120

FIG. 4

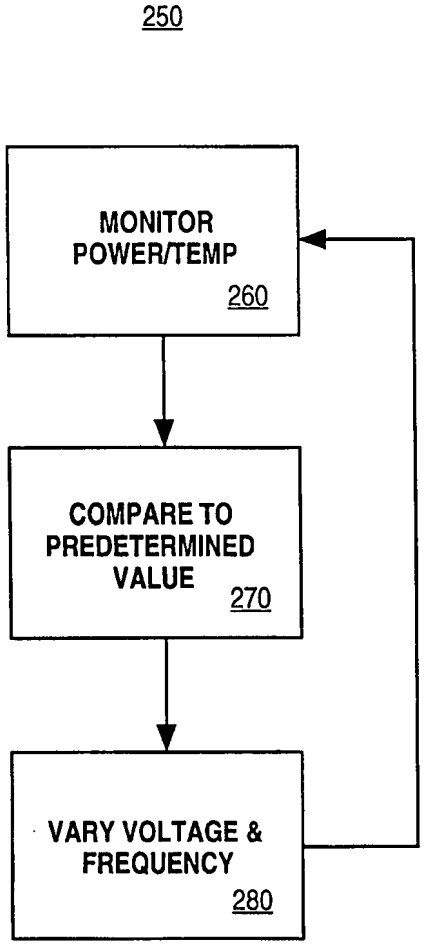
250
MONITOR POWER/TEMP
260
COMPARE TO PREDETERMINED VALUE
270
VARY VOLTAGE & FREQUENCY
280

FIG. 5

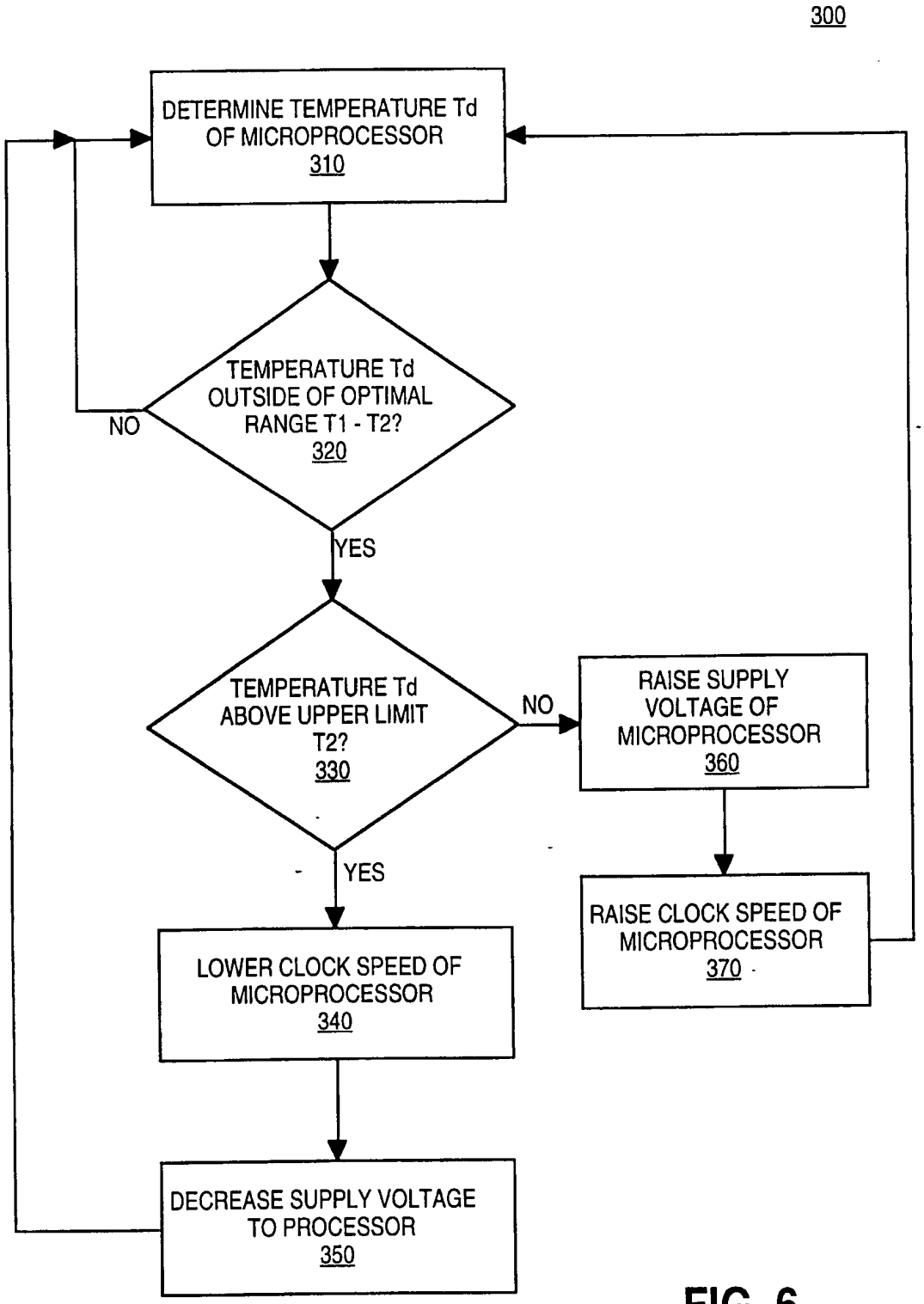
300
DETERMINE TEMPERATURE Td OF MICROPROCESSOR 310
TEMPERATURE Td OUTSIDE OF OPTIMAL RANGE T1 - T2? 320
NO
YES
TEMPERATURE Td ABOVE UPPER LIMIT T2? 330
NO
RAISE SUPPLY VOLTAGE OF MICROPROCESSOR 360
RAISE CLOCK SPEED OF MICROPROCESSOR 370
YES
LOWER CLOCK SPEED OF MICROPROCESSOR 340
DECREASE SUPPLY VOLTAGE TO PROCESSOR 350

FIG. 6

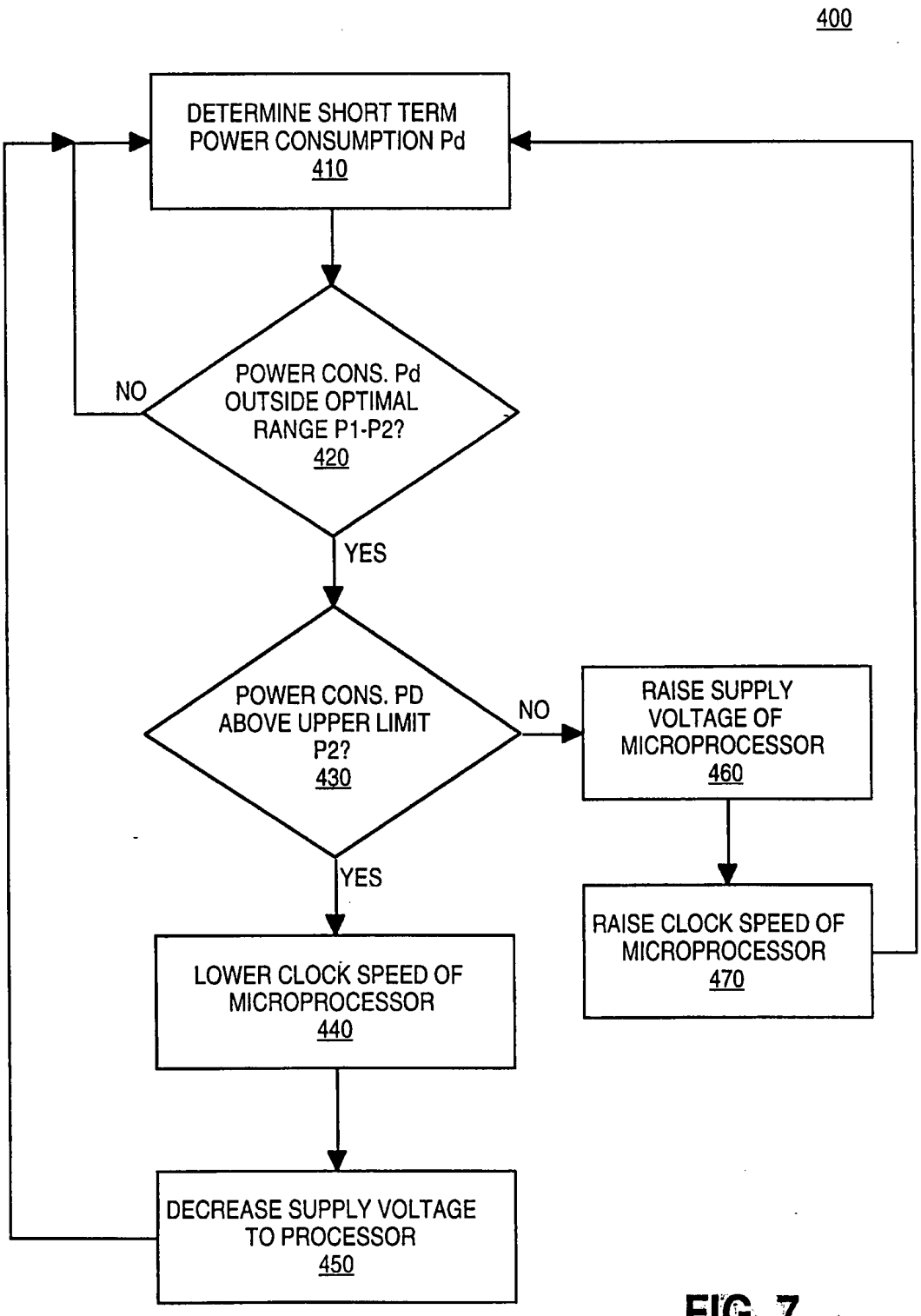
400
DETERMINE SHORT TERM POWER CONSUMPTION Pd
410
POWER CONS. Pd OUTSIDE OPTIMAL RANGE P1-P2?
420
NO
YES
POWER CONS. PD ABOVE UPPER LIMIT P2?
430
NO
RAISE SUPPLY VOLTAGE OF MICROPROCESSOR
460
YES
RAISE CLOCK SPEED OF MICROPROCESSOR
470
LOWER CLOCK SPEED OF MICROPROCESSOR
440
DECREASE SUPPLY VOLTAGE TO PROCESSOR
450

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/24194

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : G06F 1/00; G05D 23/00
US CL : 713/300, 320, 322, 340
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 713/300, 320, 322, 340; 702/132

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
STN International File uspatfull

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,719,800 A (MITTAL et al) 17 February 1998 Figure 1B, Figure 5, Column 1 lines 36-45, Column 2 line 65 to Column 3 line 50	1-24
A	US 5,560,022 A (DUNSTAN et al) 24 September 1996, ALL	1-24
A	US 5,655,127 A (RABE et al) 05 August 1997, ALL	1-24
A	US 5,291,607 A (RISTIC et al) 01 March 1994, ALL	1-24
A	US 5,339,445 A (GASZTONYI) 16 August 1994, ALL	1-24
A	US 5,726,901 A (BROWN) 10 March 1998, ALL	1-24
A	US 5,422,806 A (CHEN et al) 06 June 1995, ALL	1-24

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
07 DECEMBER 1999

Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/24194

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,367,638 A (NIESSEN et al) 22 November 1994, ALL	1-24
X,P	US 5,940,785 A (GEORGIOU et al) 17 August 1999, Title, Abstract, Figure 2	5-11, 19-24
A,P	US 5,832,284 A (MICHAIL et al) 03 November 1998, ALL	1-24
A,E	US 5,996,084 A (WATTS) 30 November 1999, ALL	1-24
A,P	US 5,940,786 A (STEEBY) 17 August 1999, ALL	1-24